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TITLE: SEMICONDUCTOR DEVICE AND ELECTRONIC COMPONENT MOUNTING THE SAME

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ABSTRACT:

PROBLEM TO BE SOLVED: To provide a technique of semiconductor device, capable of preventing a package board of the semiconductor device in which a semiconductor chip mounted on the package board is prevented from warping through bumps.

SOLUTION: A semiconductor device is formed by a package board 1 on which first and second semiconductor chips 3a and 3b, having predetermined circuit elements on it, are mounted on both sides of the board

respectively. The first
and semiconductor chips 3a and 3b are mounted opposite on the other side of the
package board 1 and connected electrically to the wiring layer through the bump
4. A plurality of solder bumps 2 electrically connecting the first and second
semiconductor chips 3a to the mounting board through the wiring layer is formed
on the package board 1.

JP 10-79405

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device with which the semiconductor chip was carried in the package substrate through the bump.
[0002]
[Description of the Prior Art] The semiconductor device carried in it is in the inclination of a miniaturization and the formation of many pins with the miniaturization of an electron and an information equipment, and multi-functionalization. Corresponding to such a tidal current, like the publication to Kogyo Chosakai Publishing Issue, "an electronic ingredient (the 1995 April issue)" (Heisei seven-year April one-day issue), and P22-P28, a semiconductor chip is carried in a package substrate through a bump, and the semiconductor device called CSP (Chip Size Package) which filled up the clearance between both with resin is known.
[0003] In order that the semiconductor device in here may connect a semiconductor chip and a package substrate, supplying to the heat treating furnace of about 250 degrees C, and fusing a bump is performed. And after bump melting, this is cooled to a room temperature.
[0004]
[Problem(s) to be Solved by the Invention] However, since a big aperture is in the coefficient of thermal expansion of a semiconductor chip and a package substrate with the above mentioned technique, it is (semiconductor chip:; 3-5 ppm /, **, and a package substrate; curvature arises in a package substrate in 17-25 ppm[/degree C]) and a cooling process. When filled up with closure resin between a semiconductor chip and a package substrate, hardening contraction of closure resin is added and this phenomenon appears much more notably.
[0005] When such a semiconductor device is connected to a mounting substrate through a solder bump etc., the variation in the height of the solder bump located between a package substrate and a mounting substrate by curvature becomes large. And by the solder bump with low height, the stress generated between the package substrate and mounting substrate in a heat cycle test etc. could not fully be eased, but there was a problem that connection dependability fell.
[0006] Then, the purpose of this invention is to offer the technique in which the curvature of the package substrate in the semiconductor device with which the semiconductor chip was carried in the package substrate through the bump can be prevented.
[0007] The other purposes and the new description will become clear from description and the accompanying drawing of this specification along [said] this invention.
[0008]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0009] Namely, as for the semiconductor device of this invention, the 1st and 2nd semiconductor chips with which the predetermined circuit element was formed are carried in each field of a package substrate. The 1st and 2nd semiconductor chips are carried in the location which faces, and are electrically connected with the wiring layer through the bump. Two or more mounting connection objects which connect electrically the 1st and 2nd semiconductor chips and mounting substrates to a package substrate through a wiring layer are formed. In such a semiconductor device, the 1st

semiconductor chip can be set to CPU and the 2nd semiconductor chip can be used as the memory controlled by this CPU.
[0010] Moreover, the semiconductor chip with which the predetermined circuit element's was formed, and this semiconductor chip and coefficient of thermal expansion of the semiconductor device of this invention being the same, or the plate material to approximate is carried in each field of a package substrate. A semiconductor chip and plate material are carried in the location which faces, and the semiconductor chip is electrically connected with the wiring layer through the bump. Two or more mounting connection objects which connect a semiconductor chip and a mounting substrate to a package substrate electrically through a wiring layer are formed. In this semiconductor device, the ceramic of boron nitride, alumimium nitride, silicon carbide, a mullite, or an alumina can be used for plate material.

[0011] Furthermore, as for the semiconductor device of this invention, the semiconductor chip and dummy chip with which the predetermined circuit element was formed are carried in each field of a package substrate. The semiconductor chip and the dummy chip are carried in the location which faces, and the semiconductor chip is electrically connected with the wiring layer through the bump. Two or more mounting connection objects which connect a semiconductor chip and a mounting substrate to a package substrate electrically through a wiring layer are formed.
[0012] And on the other hand, the concave section is formed in a field at least, and you may make it equip in these semiconductor devices, where [of a package substrate] a semiconductor chip, plate material, or a dummy chip is inserted in this concave section.
[0013] Moreover, such a semiconductor device is mounted in a mounting substrate, and the electronic parts of this invention are constituted.
[0014] According to the above-mentioned means, the stress which is going to curve a package substrate is negated and reduction of the curvature of this package substrate is attained. Moreover, it becomes possible to shorten the combination, then the signal electrical transmission path of CPU and memory in two semiconductor chips, and to attain improvement in the speed of a semiconductor device.
[0015]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail based on a drawing. In addition, in the complete diagram for explaining the gestalt of operation, the same sign is given to the same member and explanation of the repeat is omitted.
[0016] (Gestalt 1 of operation) The sectional view showing the semiconductor device whose drawing 1 is the gestalt of 1 operation of this invention, the explanatory view in which drawing 2 shows continuously an example like the erector of the semiconductor device of drawing 1 by (a) - (d), and drawing 3 are the perspective views showing the condition that the semiconductor device of drawing 1 was mounted in the mounting substrate.
[0017] The semiconductor device shown in drawing 1 is a semiconductor device of the BGA (Ball Grid Array) type which carries this in the mounting substrate 8 (drawing 3) through the solder bump (mounting connection object) 2 arranged in the shape of an array at the rear face of the package substrate 1. For example, both sides of the package substrate 1 in which it was constituted by the member which has insulation like a mullite ceramic, and the wiring layer was formed are equipped with the 1st and 2nd semiconductor chips 3a and 3b with which the predetermined circuit element was formed. Here, 1st semiconductor chip 3a is CPU (Central Processing Unit-arithmetic and program control) which performs required processing according to the read instruction, and 2nd semiconductor chip 3b has become the memory controlled by 1st semiconductor chip 3a which is CPU. However, even if reverse in the helicopter loading site of 1st semiconductor chip 3a and 2nd semiconductor chip 3b, it may be good, and you may be combination other than CPU and memory. And the helicopter loading site of these semiconductor chips 3a and 3b is a location which faces on both sides of the package substrate 1, and is electrically connected with the wiring layer through the bump 4, respectively. In addition, the bumps 4 including the gestalt of the following operations who make connection of the solder bump 2 and semiconductor chips 3a and 3b which make connection between the package substrate 1 and the mounting substrate 8, and the package substrate 1 consist of Au(gold), an Sn(tin)-Pb (lead) alloy, an Ag (silver)-Sn alloy, etc.
[0018] It is equipped with 2nd semiconductor chip 3b in the condition of having been inserted in concave section 1a formed in the rear face of the package substrate 1, the amount of protrusions is made

into two or less solder bump, and it is prevented that the solder bump 2 and the mounting substrate 8 become connection impossible by interference of 2nd semiconductor chip 3b at the time of mounting. However, when such a situation does not generate concave section 1a Making, either, concave section 1a is not necessarily required, and it forms the concave section in a front face, it is made to carry 1st semiconductor chip 3a in this, and you may make it stop the height of a semiconductor device.

[0019] Between the package substrate 1 and each semiconductor chips 3a and 3b carried in this, in order to protect a bump 4 from an external ambient atmosphere, the closure resin 5 currently generally used is filled up with the semi-conductor field. However, using what blended thermosetting resin, such as an epoxy resin, silicone resin, polyimide resin, and phenol resin, with closure resin 5 for bulking agents, such as a silica and an alumina, the hardening accelerator, the release agent, the coloring agent, the flame retarder, etc. at independence or the thing mixed two or more kinds, resin restoration of the liquefied thing can be carried out by the potting method at a room temperature, or heating melting of the solid object can be carried out at a room temperature, and resin impregnation can be carried out with a transfer system.

[0020] The semiconductor device of such a configuration is assembled through a series of processes (a) - (d) shown in drawing 2 .

[0021] first, as shown in drawing 2 (a), 1st semiconductor chip 3a in which the bump 4 was formed is doubled with the predetermined location (location which faces concave section 1a on the back here) of the front face of the package substrate 1 in which the wiring layer was formed, and a bump 4 fuses this -- for example -- It heats even to the temperature which is about 250 degrees C, and the electrode exposed to the front face from the wiring layer and 1st semiconductor chip 3a connect. After connecting both, heat hardening of the liquefied closure resin 5 is filled up with and carried out between 1st semiconductor chip 3a and the package substrate 1 (drawing 2 (b)).

[0022] Next, the process (it corresponds to drawing 2 (a) and (b)) which mentioned the package substrate 1 above in the same way as the case where inside-out and 1st semiconductor chip 3a are connected is repeated, and a rear face is equipped with 2nd semiconductor chip 3b. In addition, concave section 1a is formed in the rear face of the package substrate 1, and 2nd semiconductor chip 3b is carried in the form inserted in this concave section 1a.

[0023] And as shown in drawing 2 (c), after connecting the 1st and 2nd semiconductor chips 3a and 3b to both sides of the package substrate 1, respectively, the solder bump 2 is formed in the rear face of the package substrate 1 which is a connection side with the mounting substrate 8.

[0024] Thus, as it connects electrically and mechanically and the electrode of wiring 8a formed in the mounting substrate 8 and the bump corresponding to this show drawing 3 , surface mounting of the manufactured semiconductor device is carried out to the mounting substrate 8. This constitutes some electronic parts which consist of a mounting substrate 8 and many semiconductor devices. And transfer of a signal will be performed among other semiconductor devices by being carried in a device predetermined in an electronic-parts unit.

[0025] Thus, in the semiconductor device of the gestalt of this operation, since the 1st and 2nd semiconductor chips 3a and 3b which are the same coefficients of thermal expansion are carried in the location where both sides of the package substrate 1 face, by hardening contraction of the difference in the coefficient of thermal expansion of the package substrate 1 and semiconductor chips 3a and 3b, or closure resin 5, the stress which is going to curve the package substrate 1 is negated and reduction of the curvature of the package substrate 1 is attained. Thereby, each height of the solder bump 2 at the time of connecting a semiconductor device to the mounting substrate 8 can become the same, and can raise the connection dependability of equipment.

[0026] Moreover, by making two semiconductor chips 3a and 3b carried into the combination of CPU and memory, a signal electrical transmission path is shortened by contiguity arrangement, signal delay decreases, and it becomes possible to attain improvement in the speed of a semiconductor device.

[0027] (Gestalt 2 of operation) Drawing 4 is the sectional view showing the semiconductor device which is the gestalt of other operations of this invention.

[0028] In the semiconductor device in the gestalt of this operation, the semiconductor chip 3 with which the circuit element was formed in the front face of the package substrate 1 is connected and carried in a wiring layer through a bump 4, and the rear-face location which faces a semiconductor chip 3 is equipped with the plate material 6. It consists of this plate material 6, and the same as that of the

coefficient of thermal expansion of the semiconductor chip 3 3-5ppm/ ** or a member, for example like the ceramic of boron nitride, alumimium nitride, silicon carbide, a mullite, or an alumina to approximate. However, even if it is members other than these, using suitably is possible if a coefficient of thermal expansion is a thing 10 ppm [/degree C] or less. Moreover, the helicopter loading site of a semiconductor chip 3 and the plate material 6 may be reverse.

[0029] In addition, the assembly of the semiconductor device of the gestalt of this operation heats the same procedure as the semiconductor device explained to the above mentioned gestalt 1 of operation, i.e., a semiconductor chip 3 and the package substrate 1, is filled up with closure resin 5, equips concave section 1a with the plate material 6, and is performed by the procedure of finally forming the solder bump 2.

[0030] Also in the semiconductor device of the gestalt of this operation, since the semiconductor chip 3 and the plate material 6 which have an almost equivalent coefficient of thermal expansion mutually are carried in the location where both sides of the package substrate 1 face, the stress which is going to curve the package substrate 1 can be negated, reduction of the curvature of this package substrate 1 can be attained, and the connection dependability of equipment can be raised.

[0031] (Gestalt 3 of operation) Drawing 5 is the sectional view showing the semiconductor device of this invention which is the gestalt of other operations further.

[0032] In the semiconductor device by the gestalt of this operation, it replaces with the plate material of the above mentioned gestalt 2 of operation, and is equipped with the semiconductor chip 7 to which the wiring layer of the package substrate 1 is not connected electrically, i.e., a dummy chip.

[0033] Also in the semiconductor device of such a configuration, since this dummy chip 7 has the same coefficient of thermal expansion as a semiconductor chip 3, it becomes possible to reduce the curvature of the package substrate 1 and to raise the connection dependability of equipment.

[0034] As mentioned above, although invention made by this invention person was concretely explained based on the gestalt of the operation, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the gestalt of said operation, and does not deviate from the summary.

[0035] For example, the semiconductor device currently explained with the gestalt of this operation is able to apply this invention to other various semiconductor devices, such as PGA (Pin Grid Array) of for example, a surface mount method, although the solder bump 2 is used as a mounting connection object for BGA, and in being PGA, the lead drawn by the rear face and the perpendicular serves as a mounting connection object.

[0036]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly.

[0037] (1) According to ., i.e., this invention, the stress which is going to curve a package substrate by hardening contraction of the difference in the coefficient of thermal expansion of a package substrate and a semiconductor chip or closure resin is negated, and reduction of the curvature of a package substrate is attained. Therefore, in every part, the height of the solder bump at the time of connecting a semiconductor device to a mounting substrate can become the same, and can raise the connection dependability of equipment.

[0038] (2) By making . and two semiconductor chips carried into the combination of CPU and memory, a signal electrical transmission path is shortened, signal delay decreases, and it becomes possible to attain improvement in the speed of a semiconductor device.

[Translation done.]

* NOTICES *

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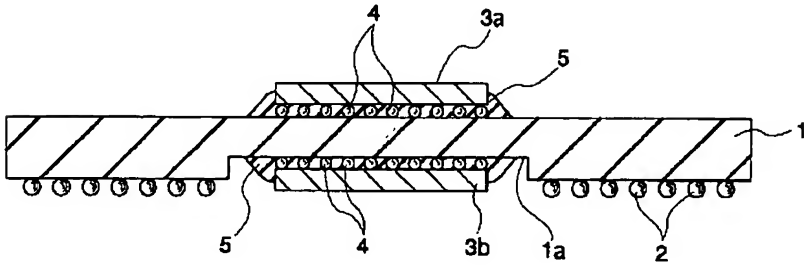
DRAWINGS

[Drawing 1]

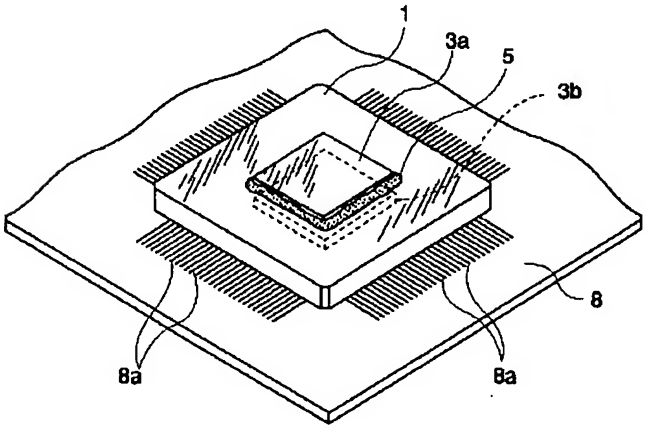
図 1



1：パッケージ基板
2：はんだバンプ
3a：第1の半導体チップ
3b：第2の半導体チップ
4：バンプ

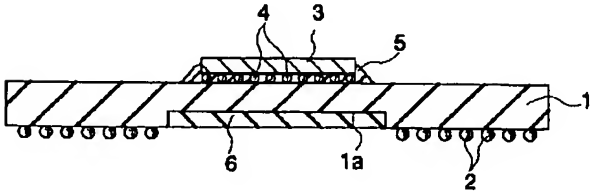
[Drawing 3]

図 3



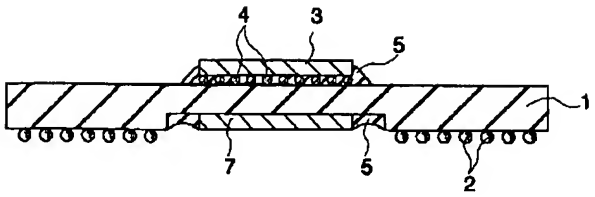
[Drawing 4]

図 4



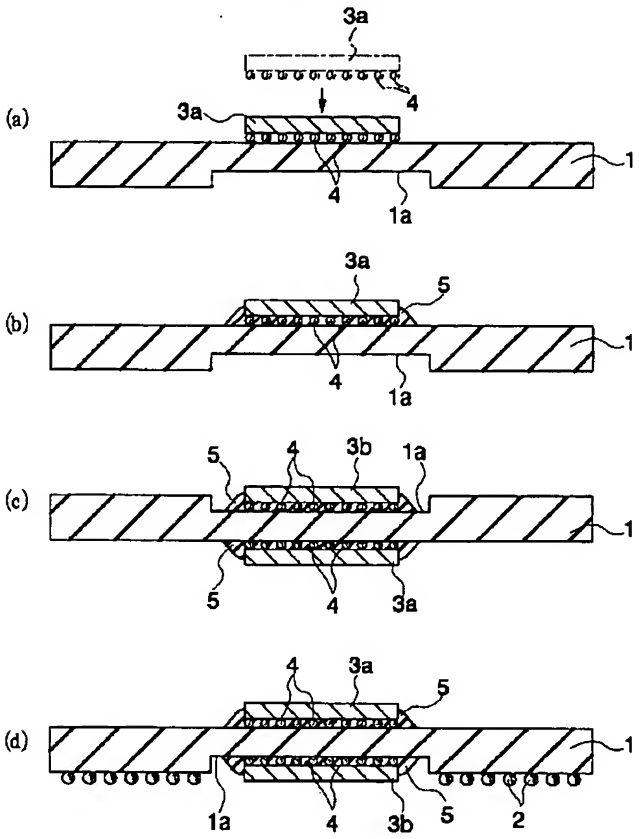
[Drawing 5]

図 5



[Drawing 2]

図 2



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CLAIMS

[Claim(s)]
[Claim 1] It is constituted by the 1st and 2nd semiconductor chips with which the predetermined circuit element was formed, and the member which has insulation, and a wiring layer is formed. In the location where said 1st and 2nd semiconductor chips face And the package substrate with which each field was equipped through the bump, respectively and which was electrically connected to this wiring layer, The semiconductor device characterized by consisting of two or more mounting connection objects which are formed in said package substrate and connect electrically said the 1st and 2nd semiconductor chips and mounting substrates through said wiring layer.
[Claim 2] It is the semiconductor device which said 1st semiconductor chip is CPU and is characterized by said 2nd semiconductor chip being memory controlled by this CPU in a semiconductor device according to claim 1.
[Claim 3] It is constituted by the semiconductor chip with which the predetermined circuit element was formed, and the member which has insulation, and a wiring layer is formed. While connecting with said wiring layer electrically through a bump and carrying said semiconductor chip in a field on the other hand, this semiconductor chip, and that a coefficient of thermal expansion is the same or the package substrate with which the location where the plate material to approximate faces said semiconductor chip of an another side side was equipped, The semiconductor device characterized by consisting of two or more mounting connection objects which are formed in said package substrate and connect said semiconductor chip and mounting substrate electrically through said wiring layer.
[Claim 4] It is the semiconductor device characterized by said plate material being the ceramic of boron nitride, alumimium nitride, silicon carbide, a mullite, or an alumina in a semiconductor device according to claim 3.
[Claim 5] It is constituted by the semiconductor chip with which the predetermined circuit element was formed, and the member which has insulation, and a wiring layer is formed. The package substrate with which the location which faces said semiconductor chip of an another side side was equipped with the dummy chip to which this wiring layer is not connected electrically while connecting with said wiring layer electrically through the bump and carrying said semiconductor chip in the field on the other hand, The semiconductor device characterized by consisting of two or more mounting connection objects which are formed in said package substrate and connect said semiconductor chip and mounting substrate electrically through said wiring layer.
[Claim 6] It is the semiconductor device which the concave section is formed in a field on the other hand at least, and is characterized by being equipped with said semiconductor chip, said plate material, or a dummy chip in the condition of said package substrate of having been inserted in this concave section in a semiconductor device according to claim 1, 2, 3, 4, or 5.
[Claim 7] Electronic parts characterized by coming to mount a semiconductor device according to claim 1, 2, 3, 4, 5, or 6 in a mounting substrate.

[Translation done.]